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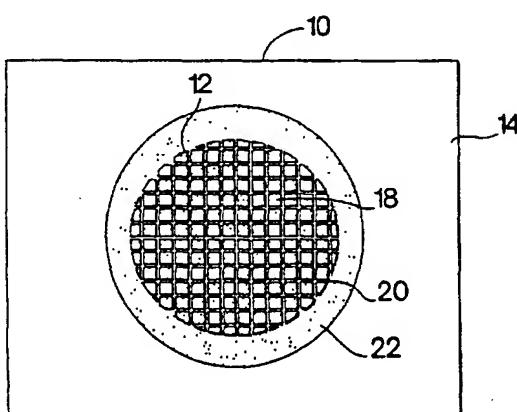
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(54) Title: WAFER COATING METHOD FOR FLIP CHIPS



(57) Abstract: A method for applying an underfill and edge coating to a flip chip is described. The method includes the steps of adhering a bumped wafer to an expandable carrier substrate, sawing the wafer to form individual chips, stretching the carrier substrate in a bidirectional manner to form channels between each of the individual chips, applying an underfill material to the bumped surfaces of the chips and around the edges of the chips, cutting the underfill material in the channels between the chips and removing the individual, underfill coated chips from the carrier.

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## WAFER COATING METHOD FOR FLIP CHIPS

### Related Applications

This application is a continuation-in-part of U.S. Application Serial Number 09/067,381,

entitled "Flip Chip With Integrated Flux and Underfill" filed April 27, 1998, and a

5 continuation-in-part of U.S. Application Serial Number 09/266,166, entitled "Flip Chip With  
Integrated Mask and Underfill" filed March 10, 1999.

### Field of the Invention

The present invention relates generally for methods of providing underfill materials on flip

10 chips. More particularly, the present invention relates to a method in which a wafer is provided with solder bumps and diced prior to the application of a polymeric underfill material.

### Background of the Invention

15 Flip chip technology, although several decades old in the ceramic module area, has recently been applied to organic substrates. Flip chip methodologies, first employed over 30 years ago, involve directly attaching Integrated Circuits (ICs) to circuit boards by means of a joint instead of a wire. This method is also called Direct Chip Attach (DCA). Several mainframe computer makers and other manufacturers of electronic components, have used this flip chip 20 technology to produce very efficient, high-density modules. The direct attachment of the ICs to circuit boards eliminates the IC component package that can occupy up to 50 times more space than the IC chip itself.

Many companies have used flip chips exclusively on ceramic circuits that have a low

25 Coefficient of Thermal Expansion (CTE). In these applications, the chip and circuit have a relatively close thermomechanical match. As a result, upon heating, the IC and the substrate upon which it is mounted undergo similar thermal expansions with the result being that physical stresses between the IC and the substrate are minimized or maintained within

acceptable limits. However, when flip chip technology is applied to the more common and considerably lower cost organic printed circuit boards, a large thermal mismatch results.

Typical organic printed circuit boards (PCBs) have a CTE of 15 to 25 parts per million per °C (ppm/°C) compared to only 2-3 ppm/°C for silicon ICs. The results are that excessive stress is generated during thermal cycling of flip chips that have been attached to PCBs. These forces can be great enough to destroy the joints that connect the chip to the circuit.

One common solution to the flip chip thermal mismatch problem has been known for some time. Specifically, a liquid polymerizable material, called an "underfill", is flowed under the

flip chip. Once the underfill has completely filled the small gap that exists between the bottom of the flip chip and the substrate, the material is hardened by polymerization. The hardened, polymerized underfill locks the flip chip and circuit board together so that there is little if any differential movement. As a result, the very rigid flip chip is mechanically coupled to the substrate by means of the underfill. Thus, the substrate expansion, at least at the interface, is restrained. This restraint causes the substrate adjacent to the flip chip to physically behave in a manner that is similar to that of the flip chip. By controlling excessive stresses that would otherwise form in the joints between the chip and PCB, a reliable assembly can be fabricated.

While the use of underfill has solved the thermal mismatch problem for low cost flip chips on organic substrates, it has given rise to a series of significant manufacturing problems. First, the prepolymerized liquid underfill must be applied off-line as a secondary process with special equipment. Typically, the underfill is applied to one, two or three edges of the assembled flip chip and allowed to flow all the way under the mounted chip. Once the

material has flowed to opposite edges and all air has been displaced from under the chip, additional underfill is dispensed to those outer edges to form a fillet so that all four edges are symmetrical. The fillet increases reliability and is generally preferred even though it requires additional manufacturing time. Next the assembly is baked in an oven to polymerize

and harden the underfill, again adding time to the process. This baking process can take several hours, although, new processes, such as microwave curing, may reduce the time substantially. However, the added equipment and its maintenance adds significantly to manufacturing costs. Thus, while the use of underfill helps to alleviate the thermal mismatch problem and provides a commercial solution, the electronic device manufacturing industry seeks more efficient manufacturing methods with lower associated costs. In fact, many in the industry believe that the present burden imposed by underfill processing may inhibit industry wide use of flip chip technology.

10 Recently, advances have been made which improve and streamline the underfill process. One method that has shown some commercial interest involves dispensing underfill before assembling the flip chip to the board. The method requires that the underfill permit solder joints to form. Soldering of flip chips to circuits is generally accomplished by applying flux to the solder bumps on the flip chip or to the circuit pads on the circuit. An underfill that is 15 pre-dispensed before soldering should contain flux or have properties that facilitate solder joint formation. Since the pads on circuit often oxidize and since tin/lead solder bumps on flip chips are always oxidized, the flux must be designed to reduce these oxide coatings and facilitate solder joint formation. These so called, pre-dispensed underfills, have therefore been designed to include flux chemistry. While simplifying the flip chip process, they still 20 require extra steps and cannot be run on a standard surface mount assembly line.

In spite of the numerous advantages provided by flip chip technology, a need still exists for flip chip methods which simplify the application of underfill. A need also exists for process methodologies which reduce the number of process steps required with underfill application.

25

#### Summary of the Invention

The present invention relates to a method for applying underfill to flip chips prior to assembling such chips on printed circuit boards. The invention is characterized in that it

simplifies the process of applying the underfill, permits conventional sawing methods to be used in singulating the wafer and provides underfill not only on the underside of each chip but along each edge of the chip as well.

5 More particularly, the present invention relates to a process which includes the steps of providing an expandable adhesive substrate having adhered thereto a wafer having solder bumps, cutting or sawing the wafer to define one or more individual integrated circuit chips, stretching the adhesive substrate in a manner which separates each individual integrated circuit from those adjacent to it, and providing an underfill material on the bumped surface  
10 and along each edge of each integrated circuit. The resulting underfill-coated chips can then be removed from the adhesive substrate and individually packaged for transport and storage until they are applied to a printed circuit.

Once positioned on a printed circuit board, the assembly is transported through a reflow oven  
15 or other means in which to heat the solder and polymerize the underfill, thereby effectively mounting the chips in place. The resulting chips are soldered into position on the printed circuit board, and include a complete underfill and surrounding polymeric fillet. Of course, if the underfill material is a prepolymerized, thermoplastic material, the heating step serves to melt the underfill, allowing it to flow and bond between the chip and the printed circuit board.  
20

#### Brief Description of the Drawings

FIG. 1 is a schematic representation of a wafer adhered to a temporary, expandable carrier substrate.

25 FIG. 2 is a schematic representation of a cut wafer adhered to a temporary, expandable carrier substrate.

FIG. 3 is a schematic representation of a cut wafer adhered to a temporary, expandable carrier substrate following stretching of the substrate.

FIG. 4 is a schematic representation of the wafer of FIG. 3 after an underfill coating has been applied to the wafer surface.

FIG. 5 is a schematic representation of a bumped flip chip having an underfill material covering its underside and edges.

5

#### Detailed Description of the Invention

This invention involves a novel coating method for applying an underfill alone, flux-in combination with an underfill, or combined flux-underfill liquids to a semiconductor wafer that has been pre-cut, or sawn, where the singulated chips are temporarily held in position by

10 an adhesive-coated film tape. The particular flux and underfill materials are described in co-pending U.S. Patent Application Serial Number 09/067,381, entitled "Flip Chip With Integrated Flux and Underfill", and in co-pending U.S. Patent Application Serial Number 09/266,166, entitled "Flip Chip With Integrated Mask and Underfill". The teachings of these co-pending patent applications are incorporated herein by reference.

15

Several benefits are provided by the present invention. First, by singulating the semiconductor wafer prior to applying the underfill material, the difficult step of sawing the wafer and the hardened integral underfill material simultaneously is avoided. Second, the invention eliminates difficulties associated with visually locating the cutting lines, (called 20 "streets"), on the wafer since sawing is carried out before application of underfill material. Third, the present invention yields chips having underfill coating each of their four edges. This edge coating provides the additional underfill material needed to form edge fillets during the solder reflow process. As noted above, fillets have been shown to increase the performance of underfill.

25

The invention is a multi-step process which can be described as follows. An uncut wafer having solder bumps provided on one surface is adhered to a temporary, expandable adhesive-coated carrier film. One preferred film of this type is commonly referred to as

“Nitto Tape” (commercially available from Nitto-Denko, Ltd.). Once the wafer has been adhered to the carrier film, it is cut into individual chips in a process referred to as “singulation”. Cutting is commonly achieved using a precision saw which is designed to make a narrow cut having clean edges. Additionally, the cutting process must be one which does not cut through the carrier substrate. Rather, the singulation is carried out in a manner that divides the wafer into individual chips, while leaving the carrier film intact. Following singulation, the tape is stretched or expand in a controlled, multidirectional manner. In so doing, the individual chips, while remaining adhered to the carrier substrate, are separated from each other, and spaces or channels are formed between them. To this point, the process described above is substantially the same as those currently known in the art.

10

The inventive portion of the process occurs following stretching of the carrier substrate and the related separation of the individual chips. Specifically, the separated chips, while still adhered to the carrier, are coated with the underfill material. In embodiments in which flux is necessary and is applied separately, the flux can be applied at this stage as well.

15 Alternatively, in embodiments employing a flux-containing underfill or an underfill having fluxing properties, just the underfill material is applied to the wafer. The underfill is applied in a manner such that it covers the bumped surface to an appropriate depth (depending upon its fluxing characteristics) and also in a manner such that it surrounds the edges of each 20 singulated chip. As discussed above, this edge coating provides desirable properties to the resulting fillet upon curing of the underfill material.

20

Once the underfill material has been applied to the bumped surface of each chip and its edges, it is caused or allowed to dry, and then the dried coating that lies in the spaces or channels 25 between each chip is cut to thereby separate each coated chip for packaging and subsequent processing.

As noted previously, the steps of mounting a wafer on an expandable, adhesive carrier substrate, cutting the wafer into singulated chips, and then expanding the adhesive carrier substrate to isolate the individual chips from one another is well-known in the art. These steps are done routinely in the semiconductor and packaging fields. Equipment for carrying

5 out these steps is available from several suppliers (such as Hover-Davis). This equipment typically is designed to stretch the carrier tape equally so that the space between the chips is approximately equal. This is normally done to permit easy chip removal from the tape without damaging chip edges as the chips are "picked" off the carrier. Unlike the prior art, one consideration of the present invention is to provide a controlled, preferably uniform, 10 spacing that will become filled with liquid underfill material during the coating process. One method for adjusting the amount of underfill material applied to each chip is to alter the spacing between each chip. This adjustment is useful because the thickness of the underfill coating applied to the wafer will vary with the type of flip chips and their bump height.

15 As noted above, once the adhered wafer has been cut into individual chips and the spacing between those chips has been achieved to the desired value via stretching of the carrier, the underfill material can be applied. The incorporated applications describe two different flux-underfill systems, each of which employs a different set of coating steps when used in connection with the process of the present invention.

20 The process described above may be best understood with reference to the Figures. In FIG. 1, the adhered workpiece 10 comprises a bumped wafer 12 adhered to a surface of a temporary, expandable carrier substrate. As shown in FIG. 2, the wafer 12, while still adhered to the carrier substrate 14 has been sawed or cut along several pathways 16 to define a plurality of 25 individual bumped chips 18. Following the cutting, the substrate 14 is stretched, as shown in FIG. 3, to isolate or singulate the individual flip chips 18 by forming spaces or channels 20 between them. In FIG. 4, the workpiece 10 has then been coated with the underfill material 22 which covers both the singulated chips 18 as well as the channels 20 between such chips.

The underfill material 22 occupying the channels 20 is then cut and the individual underfill coated chips can be removed and packaged.

One such chip is shown schematically in FIG. 5. In FIG. 5, the underfilled, bumped chip 24 includes a singulated integrated circuit chip 18 having solder bumps 26 on its underside. An underfill coating has been provided in a manner such that it covers the underside of the chip (22a) and also extends a short distance beyond the edges of the chip (22b) in order to effectively provide a fillet having underfill which entirely surrounds the edge of the chip as well as coating the underside of the chip.

10

A two-component system having a separate flux and underfill composition, has been described in the previously incorporated application USSN 09/067,381. In the two-component flux and underfill composition embodiment of the invention, the flux may be applied before the underfill by a dipping process. While dipping can be prior to sawing the bumped wafer, a preferred method is to apply the flux after the wafer has been sawed in order to avoid contamination of the flux by particles of silicon which may result from the cuts. The flux can be applied before or after the carrier substrate is stretched to isolate the individual chips. However, for large wafers, it is desirable to apply flux to the bumps before sawing so that high planarity is maintained. Furthermore, to be effective, flux only needs to be applied to the bumps, rather than to the entire underside of the flip chip, and this can be done using rolling or by dipping methods. The flux is allowed to dry on or entirely around the solder bumps.

15

The workpiece, comprising the sawed and flux coated wafer adhered to the carrier substrate, is now expanded or stretched via stretching of the carrier substrate to the give the desired spacing between chips. The stretching is preferably bidirectional to achieve the appropriate spacing between each chip. In some embodiments, this stretching may have been performed

prior to the application of the flux, while in other embodiments, the stretching may occur after the application of the flux.

It should be noted that the flux described preferably has a low surface energy. As such, the  
5 flux resists over-coating by the underfill. Of course, as an alternative, the flux can be applied after the underfill has been coated and dried. It is noted that when employing an embodiment in which the flux and the underfill are separate compositions, the method used to provide the flux coating should only apply flux to the bumps, most preferably to the top surface of the bumps, since flux is not needed on the sides of the chip.

10

The underfill liquid is now ready to be applied. It is preferred that the coating methods produce a symmetrical deposition. Such methods include, but are not limited to, stencil printing, curtain coating and spraying. Spin coating, although possible, is generally not recommended because "shadowing" of cuts that are perpendicular to spin-induced flow  
15 direction may be deficient in material and the final coating may not be of uniform thickness. Once the underfill material has been applied, it is heated in order to dry the underfill coating. Heating is generally conducted for a period of time sufficient to bake out the solvent contained in the underfill material.

20

Dried coating contained in the channels between the singulated chips is then cut in order to separate the chips. This separation can be done with a wafer saw since the hardened underfills generally comprise high melting engineering thermoplastics with good sawing characteristics. Laser cutting can also be used, as can a numerically controlled knife cutting (NC knife). It is preferred that the carrier substrate not be cut through since chip removal is  
25 much easier if the tape remains as a single film.

A one-component coating system, having a combined flux and underfill composition, is described in the previously incorporated application USSN 09/266,166.

The same underfill coating methods as just described for the underfill portion of the two-component composition can be used for the one-component flux-underfill system. The cutting method for the dried material is also the same.

- 5 Following application of the coating to the underside of the chip and around its edges, the chips can be assembled to printed circuit boards using reflow soldering methods. The specifics of such assembly have been described in the previously incorporated applications. Of course, prior to use, the chips must be removed from the carrier substrate, and such chips are typically then stored in waffle packs or other standard presentation holders. The same
- 10 equipment manufacturers that sell expanding (i.e., stretching) equipment offer machines that can pick up and place chips from the substrate. The common mechanism is to pull on the chip with a vacuum tool while simultaneously pushing against the back of the substrate with an "ejector" pin.
- 15 Upon exposing the inventive chips to reflow soldering, they will become soldered to a printed circuit board while simultaneously being provided with an underfill material positioned both between the chip and the printed circuit board, as well as around the edges of the chip. The edge coating is desirable because during the reflow heating, the underfill, being thermoplastic, softens or melts to form a fillet around the attached flip chip. The fillet improves bond strength and reduces stresses, particularly thermally-induced stresses, at the edge of the chip.
- 20

#### Equivalents

From the foregoing detailed description of the specific embodiments of the invention, it should be apparent that a novel heat transfer label and heat transfer labeling system has been described. Although particular embodiments have been disclosed herein in detail, this has been done by way of example for purposes of illustration only, and is not intended to be limiting with respect to the scope of the appended claims which follow. In particular, it is

contemplated by the inventor that various substitutions, alterations, and modifications may be made to the invention without departing from the spirit and scope of the invention as defined by the claims.

CLAIMS

What is claimed is:

1. A method for providing an underfill material on an integrated circuit chip which  
5 comprises the steps of:
  - a) providing a wafer containing at least one integrated circuit chip, the integrated circuit chip having at least solder bump provided on an exposed surface thereof;
  - b) affixing the wafer to an expandable carrier substrate in a manner such that the bumped surface of the integrated circuit chip is exposed;
  - c) cutting the wafer in a manner which defines edges on said at least one integrated circuit chip, the cutting being of a depth which does not cut the carrier substrate;
  - d) expanding the carrier substrate in a manner which singulates said at least one integrated circuit chip, the singulation forming channels which surround the integrated circuit chip;
  - e) providing an underfill material on the bumped surface of the integrated circuit chip and in the channels defined by the edges of the integrated circuit chip; and
  - f) cutting the underfill contained in the channels to thereby define at least one bumped integrated circuit chip having an underfill material provided on its bumped surface and surrounding its edges.
- 10  
15  
20  
25  
2. The method of claim 1, wherein at least the said at least one solder bump is provided with a flux material.
3. The method of claim 2, wherein the flux is provided by the underfill material.
4. The method of claim 2, wherein the flux is provided in an additional process step.

5. The method of claim 4, wherein the flux is provided before the carrier substrate is expanded.
6. The method of claim 1 wherein the expansion of the carrier substrate is a bidirectional  
5 expansion.
7. The method of claim 1, wherein the underfill material is provided to a depth which allows the at least one solder bump to be exposed.
- 10 8. The method of claim 1, wherein the underfill material covers the at least one solder bump.
9. A method for providing an underfill material on an integrated circuit chip which comprises the steps of:
  - a) providing at least one integrated circuit chip adhered to a temporary carrier  
15 substrate, the integrated circuit chip having an exposed surface and a plurality of edges, the exposed surface having at least one solder bump thereon; and
  - b) providing an underfill material on the bumped surface of the integrated circuit chip and on its edges.
- 20 10. The method of claim 9, wherein at least the said at least one solder bump is provided with a flux material.
11. The method of claim 10, wherein the flux is provided by the underfill material.
- 25 12. The method of claim 10, wherein the flux is provided in an additional process step.
13. The method of claim 9, wherein the underfill material is provided to a depth which allows the at least one solder bump to be exposed.

14. The method of claim 9, wherein the underfill material covers the at least one solder bump.

15. A workpiece which comprises a plurality of integrated circuit chips, each integrated

5       circuit chip having an exposed surface with at least one solder bump thereon, the chips  
removably adhered to a carrier substrate in a manner such that channels are defined  
between the integrated circuit chips, wherein the bumped surfaces and the channels are  
provided with a coating of an underfill material.

10      16. The workpiece of claim 15, wherein at least the said at least one solder bump is provided  
with a flux material.

17. The workpiece of claim 15, wherein the underfill material is provided to a depth which  
allows the at least one solder bump to be exposed.

15

18. The workpiece of claim 15, wherein the underfill material covers the at least one solder  
bump.

19. An integrated circuit chip having a first surface, a second surface and at least one edge,  
20       wherein the first surface is adhered to a temporary carrier substrate and the second surface  
includes at least one solder bump, and further wherein an underfill material covers the  
second surface and each of said at least one edges.

20. The integrated circuit chip of claim 19, wherein at least the said at least one solder bump  
25       is provided with a flux material.

21. The integrated circuit chip of claim 19, wherein the underfill material is provided to a  
depth which allows the at least one solder bump to be exposed.

22. The integrated circuit chip of claim 19, wherein the underfill material covers the at least one solder bump.
- 5      23. A workpiece which comprises a carrier substrate having a plurality of bumped integrated circuit chips removably adhered thereto, the chips separated from one another by a plurality of channels, characterized in that the bumped integrated circuit chips and the channels include a coating of an underfill material.
- 10     24. The workpiece of claim 24 further characterized in that the coating of underfill material in the channels has been cut in a manner which isolates the underfill material coating each integrated circuit chip.

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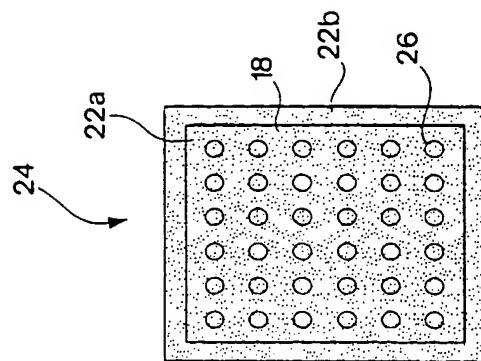


Fig. 5

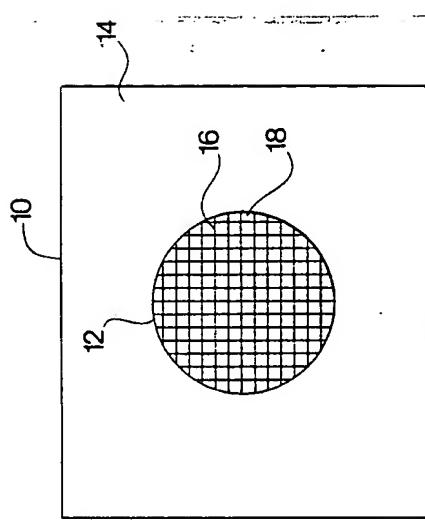


Fig. 2

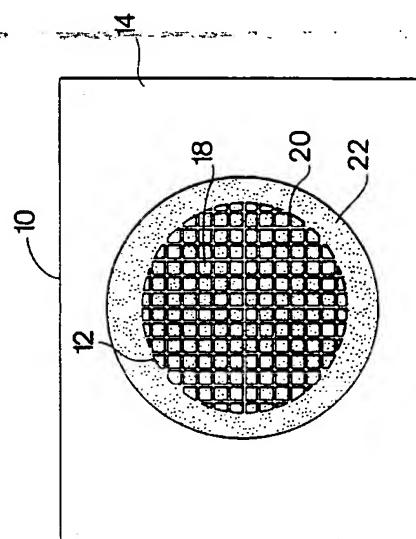


Fig. 4

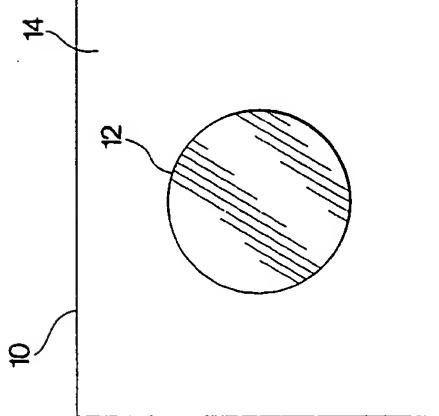


Fig. 1

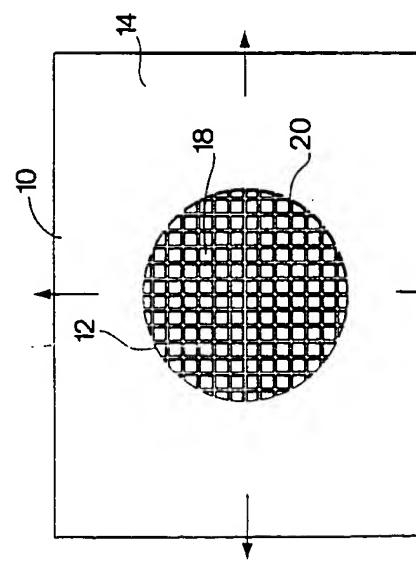


Fig. 3

## INTERNATIONAL SEARCH REPORT

Int. Application No  
PCT/US 00/25133

**A. CLASSIFICATION OF SUBJECT MATTER**  
IPC 7 H01L21/56

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)  
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

PAJ, EPO-Internal

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	<p>PATENT ABSTRACTS OF JAPAN vol. 1999, no. 09, 30 July 1999 (1999-07-30) -&amp; JP 11 121507 A (OKI ELECTRIC IND CO LTD), 30 April 1999 (1999-04-30)</p> <p>the whole document -&amp; US 5 989 982 A (TAKAHASHI YOSHIKAZU) 23 November 1999 (1999-11-23) the whole document</p> <p>----</p> <p>-/-</p>	<p>1,2,6,7, 9,10,12, 13, 15-17, 19-21, 23,24</p>

Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

\* Special categories of cited documents :

- 'A' document defining the general state of the art which is not considered to be of particular relevance
- 'E' earlier document but published on or after the international filing date
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- 'O' document referring to an oral disclosure, use, exhibition or other means
- 'P' document published prior to the international filing date but later than the priority date claimed

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Date of the actual completion of the international search

11 January 2001

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17/01/2001

Name and mailing address of the ISA

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# INTERNATIONAL SEARCH REPORT

International Application No

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**C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT**

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 1996, no. 07, 31 July 1996 (1996-07-31) -& JP 08 070081 A (NIPPONDENSO CO LTD), 12 March 1996 (1996-03-12) abstract; figure 4	1,6,7,9, 13,15, 19,21, 23,24
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